CLAIMS

What is claimed is:

1. An SRAM memory cell comprising:

a first pull-up transistor having a first substrate, a first source, a first gate coupled to a first node, and a first drain coupled to a second node, said first source being coupled to a first voltage input through parasitic resistance of said first substrate;

a first pull-down transistor having a second drain coupled to said second node, a second gate coupled to said first node, and a second source coupled to a second voltage source; and

an input line coupled to said first node for providing a signal to said memory cell to change said memory cell from a first logic state to a second logic state.

2. The memory cell of claim 1, wherein said input line comprises an access transistor having one terminal coupled to said first node, another terminal coupled to a column line and an access gate coupled to a row line.

3. An SRAM memory cell comprising:

a first pull-up transistor having a first substrate, a first source, a first gate coupled to a first node, and a first drain coupled to a second node, said first source being coupled to a first voltage input through parasitic resistance of said first substrate;

a first pull-down transistor having a second drain coupled to said second node, a second gate coupled to said first node, and a second source coupled to a second voltage input;

a second pull-up transistor having a second substrate, a third source, a third gate coupled to said second node, and a third drain coupled to said first node, said third source being coupled to said first voltage input through parasitic resistance of said second substrate;

a second pull-down transistor having a fourth drain coupled to said first node, a fourth gate coupled to said second node, and a fourth source coupled to said second voltage input; and

an input line coupled to said first and second nodes for providing a signal to said memory cell to change said memory cell from a first logic state to a second logic state.

4. The memory cell of claim 3, wherein said first substrate and said second substrate are portions of a single substrate.

5. An SRAM memory cell comprising:

a substrate assembly having at least one semiconductor layer;

a first semiconductor structure formed within said at least one semiconductor layer, said first semiconductor structure being coupled to a first voltage input;

a first pull-up transistor formed in said first semiconductor structure, said first pull-up transistor comprising a first gate, a first source and a first drain, said first source being coupled to said first semiconductor structure such that said first source is coupled to said first voltage input through parasitic resistance of said semiconductor structure; and

a first pull-down transistor formed in said at least one semiconductor layer, said first pull-down transistor comprising a second gate coupled to said first gate, a second source coupled to a second voltage input, and a second drain coupled to said first drain.

6. The memory cell of claim 5, further comprising an access transistor formed in said at least one semiconductor layer having one terminal coupled to said first and second drains, another terminal coupled to a column line and an access gate coupled to a row line.

7. The memory cell of claim 5, wherein said at least one semiconductor layer comprises P-type semiconductor material, and wherein said semiconductor structure comprises an N-type well.

8. An SRAM memory cell comprising:

a substrate assembly having at least one semiconductor layer;

a first semiconductor structure and a second semiconductor structure formed within said at least one semiconductor layer, said first and second semiconductor structures being coupled to a first voltage input;

a first pull-up transistor formed in said first semiconductor structure, said first pull-up transistor comprising a first gate, a first source and a first drain, said first source being coupled to said first semiconductor structure such that said first source is coupled to said first voltage input through parasitic resistance of said first semiconductor structure;

a first pull-down transistor formed in said at least one semiconductor layer, said first pull-down transistor comprising a second gate coupled to said first gate, a second source coupled to a second voltage input, and a second drain coupled to said first drain;

a second pull-up transistor formed in said second semiconductor structure, said second pull-up transistor comprising a third gate, a third source and a third drain, said third source being coupled to said second semiconductor structure such that said third source is coupled to said first voltage input through parasitic resistance of said second semiconductor structure; and

a second pull-down transistor formed in said at least one semiconductor layer, said second pull-down transistor comprising a fourth gate coupled to said third gate, a fourth source coupled to said second voltage input, and a fourth drain coupled to said third drain.

9. The memory cell of claim 8, wherein said at least one semiconductor layer comprises P-type semiconductor material, and wherein said first and second semiconductor structures each comprise an N-type well.

10. The memory cell of claim 8, wherein said first semiconductor structure and said second semiconductor structure form portions of a single semiconductor structure.

11. The memory cell of claim 10, wherein said at least one semiconductor layer comprises P-type semiconductor material, and wherein said first semiconductor structure comprises an N-type well.

12. The memory cell of claim 8, further comprising:

a first access transistor formed in said at least one semiconductor layer having a first terminal coupled to said first and second drains, a second terminal coupled to a first column line and a first access gate coupled to a row line; and

a second access transistor formed in said at least one semiconductor layer having a third terminal coupled to said third and fourth drains, a fourth terminal coupled to a second column line and a second access gate coupled to said row line.

13. An SRAM memory array comprising:

a plurality of memory cells arranged in rows and columns, each of said memory cells comprising:

a first pull-up transistor having a first substrate, a first source, a first gate coupled to a first node, and a first drain coupled to a second node, said first source being coupled to a first voltage input through parasitic resistance of said first substrate;

a first pull-down transistor having a second drain coupled to said second node, a second gate coupled to said first node, and a second source coupled to a second voltage input;

a second pull-up transistor having a second substrate, a third source, a third gate coupled to said second node, and a third drain coupled to said first node, said third source being coupled to said first voltage input through parasitic resistance of said second substrate;

a second pull-down transistor having a fourth drain coupled to said first node, a fourth gate coupled to said second node, and a fourth source coupled to said second voltage input;

a first access transistor having a first terminal coupled to said first and second drains, a second terminal coupled to a first column line and a first access gate coupled to a row line;

a second access transistor having a third terminal coupled to said third and fourth drains, a fourth terminal coupled to a second column line and a second access gate coupled to said row line; and

a memory decoder coupled to said plurality of memory cells for accessing each of said plurality of memory cells via said respective ones of a plurality of said row lines and respective ones of a plurality of said first and second column lines.

14. The memory array of claim 13, wherein said first substrate and said second substrate form portions of a single substrate.

15. The memory array of claim 14, wherein said memory array comprises a plurality of said rows, and wherein each of said first and second pull-up transistors making up each of said rows of memory cells share a common substrate.

16. An SRAM memory array comprising:

a plurality of SRAM memory cells arranged in rows and columns and formed on a substrate assembly comprising at least one semiconductor layer, each of said plurality of memory cells comprising:

a first semiconductor structure and a second semiconductor structure formed within said at least one semiconductor layer, said first and second semiconductor structures being coupled to a first voltage input;

a first pull-up transistor formed in said first semiconductor structure, said first pull-up transistor comprising a first gate, a first source and a first drain, said first source being coupled to said first semiconductor structure such that said first source is coupled to said first voltage input through parasitic resistance of said first semiconductor structure;

a first pull-down transistor formed in said at least one semiconductor layer, said first pull-down transistor comprising a second gate coupled to said first gate, a second source coupled to a second voltage input, and a second drain coupled to said first drain;

a second pull-up transistor formed in said second semiconductor structure, said second pull-up transistor comprising a third gate, a third source and a third drain, said third source being coupled to said second semiconductor structure such that said third source is coupled to said first voltage input through parasitic resistance of said second semiconductor structure;

a second pull-down transistor formed in said at least one semiconductor layer, said second pull-down transistor comprising a fourth gate coupled to said third gate, a fourth source coupled to said second voltage input, and a fourth drain coupled to said third drain;

a first access transistor formed in said at least one semiconductor layer having a first terminal coupled to said first and second drains, a second terminal coupled to a first column line and a first access gate coupled to a row line;

a second access transistor formed in said at least one semiconductor layer having a third terminal coupled to said third and fourth drains, a fourth terminal coupled to a second column line and a first access gate coupled to a row line; and

a memory decoder coupled to said plurality of memory cells for accessing each of said plurality of memory cells via respective ones of a plurality of said row lines and respective ones of a plurality of said first and second column lines.

17. The memory array of claim 16, wherein said first substrate and said second substrate form portions of a single substrate.

18. The memory array of claim 17, wherein said at least one semiconductor layer comprises P-type semiconductor material, and wherein said first semiconductor structure comprises an N-type well.

19. The memory array of claim 18, wherein said memory array comprises a plurality of said rows, and wherein each of said first and second pull-up transistors making up each of said rows of memory cells share said N-type well.

20. A computer system comprising:

a memory array, said memory array comprising:

a plurality of memory cells arranged in rows and columns, each of said memory cells comprising:

a first pull-up transistor having a first substrate, a first source, a first gate coupled to a first node, and a first drain coupled to a second node, said first source being coupled to a first voltage input through parasitic resistance of said first substrate;

a first pull-down transistor having a second drain coupled to said second node, a second gate coupled to said first node, and a second source coupled to a second voltage input;

a second pull-up transistor having a second substrate, a third source, a third gate coupled to said second node, and a third drain coupled to said first node, said third source being coupled to said first voltage input through parasitic resistance of said second substrate;

a second pull-down transistor having a fourth drain coupled to said first node, a fourth gate coupled to said second node, and a fourth source coupled to said second voltage input;

a first access transistor having a first terminal coupled to said first and second drains, a second terminal coupled to a first column line and a first access gate coupled to a row line;

a second access transistor having a third terminal coupled to said third and fourth drains, a fourth terminal coupled to a second column line and a second access gate coupled to said row line;

a memory decoder coupled to said plurality of memory cells for accessing each of said plurality of memory cells via respective ones of a plurality of said row lines and respective ones of a plurality of said first and second column lines; and

a microprocessor in communication with each of said plurality of memory cells via said memory decoder.

31. A computer system comprising:

a memory array formed on a substrate assembly comprising at least one semiconductor layer, said memory array comprising:

a plurality of memory cells arranged in rows and columns, each of said memory cells comprising:

a first semiconductor structure and a second semiconductor structure formed within said at least one semiconductor layer, said first and second semiconductor structures being coupled to a first voltage input;

a first pull-up transistor formed in said first semiconductor structure, said first pull-up transistor comprising a first gate, a first source and a first drain, said first source being coupled to said first semiconductor structure such that said first source is coupled to said first voltage input through parasitic resistance of said first semiconductor structure;

a first pull-down transistor formed in said at least one semiconductor layer, said first pull-down transistor comprising a second gate coupled to said first gate, a second source coupled to a second voltage input, and a second drain coupled to said first drain;

a second pull-up transistor formed in said second semiconductor structure, said second pull-up transistor comprising a third gate, a third source and a third drain, said third source being coupled to said second semiconductor structure such that said third source is coupled to said first voltage input through parasitic resistance of said second semiconductor structure;

a second pull-down transistor formed in said at least one semiconductor layer, said second pull-down transistor comprising a fourth gate coupled to said third gate, a fourth source coupled to said second voltage input, and a fourth drain coupled to said third drain;

a first access transistor formed in said at least one semiconductor layer having a first terminal coupled to said first and second drains, a second terminal coupled to a first column line and a first access gate coupled to a row line;

a second access transistor formed in said at least one semiconductor layer having a third terminal coupled to said third and fourth drains, a fourth terminal coupled to a second column line and a first access gate coupled to a row line;

a memory decoder coupled to said plurality of memory cells for accessing each of said plurality of memory cells via said respective ones of a plurality of said row lines and respective ones of a plurality of said first and second column lines; and

a microprocessor in communication with each of said plurality of memory cells via said memory decoder.

32. A method of fabricating an SRAM memory cell comprising the steps of:

providing a substrate assembly having at least one semiconductor layer;

forming a first semiconductor structure within said at least one semiconductor layer;

forming a first source and a first drain of a first pull-up transistor in said first semiconductor structure;

forming a second source and a second drain of a first pull-down transistor in said at least one semiconductor layer;

forming a first contact and a second contact within said first semiconductor structure;

forming a first gate for said first pull-up transistor and a second gate for said first pull-down transistor;

coupling said first drain to said second drain;

coupling said first gate to said second gate; and

coupling said first source to one of said first and second contacts such that with the other of said first and second contacts coupled to a first voltage input said first source is coupled to said first voltage input through parasitic resistance of said first semiconductor structure.

33. A method of fabricating an SRAM memory cell comprising the steps of:

providing a substrate assembly having at least one semiconductor layer;

forming a first semiconductor structure and a second semiconductor structure within said at least one semiconductor layer;

forming a first source and a first drain of a first pull-up transistor in said first semiconductor structure;

forming a second source and a second drain of a first pull-down transistor in said at least one semiconductor layer;

forming a third source and a third drain of a second pull-up transistor in said second semiconductor structure;

forming a fourth source and a fourth drain of a second pull-down transistor in said at least one semiconductor layer;

forming a first contact and a second contact within said first semiconductor structure;

forming a third contact and fourth contact within said second semiconductor structure;

forming a first gate for said first pull-up transistor, a second gate for said first pull-down transistor, a third gate for said second pull-up transistor and a fourth gate for said second pull-down transistor;

coupling said first drain to said second drain and said third drain to said fourth drain;

coupling said first gate to said second gate and said third gate to said fourth gate;

coupling said first source to one of said first and second contacts such that with the other of said first and second contacts coupled to a first voltage input said first source is coupled to said first voltage input through parasitic resistance of said first semiconductor structure; and

coupling said third source to one of said third and fourth contacts such that with the other of said third and fourth contacts coupled to said first voltage input said third

source is coupled to said first voltage input through parasitic resistance of said second semiconductor structure.

34. The method of claim 33, wherein said first substrate and said second substrate form portions of a single substrate.

35. The method of claim 34, wherein said at least one semiconductor layer comprises P-type semiconductor material, and wherein said first semiconductor structure comprises an N-type well.

36. The method of claim 33, wherein said at least one semiconductor layer comprises P-type semiconductor material, and wherein each of said first and second semiconductor structures comprise an N-type well.

37. A method of fabricating an SRAM memory array comprising:

providing a substrate assembly having at least one semiconductor layer;

forming a plurality of memory cells arranged in rows and columns, each of said plurality of memory cells fabricated according to the following steps:

forming a first semiconductor structure within said at least one semiconductor layer;

forming a second semiconductor structure within said at least one semiconductor layer;

forming a first source and a first drain of a first pull-up transistor in said first semiconductor structure;

forming a second source and a second drain of a first pull-down transistor in said at least one semiconductor layer;

forming a third source and a third drain of a second pull-up transistor in said second semiconductor structure;

forming a fourth source and a fourth drain of a second pull-down transistor in said at least one semiconductor layer;

forming a first terminal and a second terminal of a first access transistor in said at least one semiconductor layer;

forming a third terminal and a fourth terminal of a second access transistor in said at least one semiconductor layer;

forming a first contact and a second contact within said first semiconductor structure;

forming a third contact and fourth contact within said second semiconductor structure;

forming a first gate for said first pull-up transistor, a second gate for said first pull-down transistor, a third gate for said second pull-up transistor, a fourth gate for said second pull-down transistor, a first access gate for said first access transistor, and a second access gate for said second access transistor;

coupling said first drain to said second drain and said third drain to said fourth drain;

coupling said first gate to said second gate and said third gate to said fourth gate;

coupling said first terminal to said first and second drains;

coupling said third terminal to said third and fourth drains;

coupling said first source to one of said first and second contacts such that with the other of said first and second contacts coupled to a first voltage input said first source is coupled to said first voltage input through parasitic resistance of said first semiconductor structure;

coupling said third source to one of said third and fourth contacts such that with the other of said third and fourth contacts coupled to said first voltage input said third source is coupled to said first voltage input through parasitic resistance of said second semiconductor structure;

coupling said first and second access gates of each of said plurality of memory cells to respective row lines;

coupling said second terminals of each of said plurality of memory cells to respective first column lines; and

coupling said fourth terminals of each of said plurality of memory cells to respective second column lines.

38. The method of claim 37, wherein said first substrate and said second substrate form portions of a single substrate.

39. The method of claim 38, wherein each of said first and second pull-up transistors making up each of said rows of memory cells share said N-type well.

40. A method of fabricating a computer system comprising the steps of:

providing a memory array formed on a substrate assembly comprising at least one semiconductor layer, said memory array comprising:

a plurality of memory cells arranged in rows and columns, each of said memory cells comprising:

a first semiconductor structure and a second semiconductor structure formed within said at least one semiconductor layer, said first and second semiconductor structures being coupled to a first voltage input;

a first pull-up transistor formed in said first semiconductor structure, said first pull-up transistor comprising a first gate, a first source and a first drain, said first source being coupled to said first semiconductor structure such that said first source is coupled to said first voltage input through parasitic resistance of said first semiconductor structure;

a first pull-down transistor formed in said at least one semiconductor layer, said first pull-down transistor comprising a second gate coupled to said first gate, a second source coupled to a second voltage input, and a second drain coupled to said first drain;

a second pull-up transistor formed in said second semiconductor structure, said second pull-up transistor comprising a third gate, a third source and a third drain, said third source being coupled to said second semiconductor structure such that said third source is coupled to said first voltage input through parasitic resistance of said second semiconductor structure;

a second pull-down transistor formed in said at least one semiconductor layer, said second pull-down transistor comprising a fourth gate coupled to said third gate, a fourth source coupled to said second voltage input, and a fourth drain coupled to said third drain;

a first access transistor formed in said at least one semiconductor layer having a first terminal coupled to said first and second drains, a second terminal coupled to a first column line and a first access gate coupled to a row line;

a second access transistor formed in said at least one semiconductor layer having a third terminal coupled to said third and fourth drains, a fourth terminal coupled to a second column line and a first access gate coupled to a row line;

a memory decoder coupled to said plurality of memory cells for accessing each of said plurality of memory cells via respective ones of a plurality of said row lines and respective ones of a plurality of said first and second column lines; and

providing a microprocessor in communication with each of said plurality of memory cells via said memory decoder.